

LISTING OF THE CLAIMS:

Claims 1-20 (cancelled).

21. (New) A method for production of an encapsulated encapsulation for an electrical component comprising the steps of attaching a component with metallizations fashioned on a chip to a substrate that has electrical connection areas so that the surface of the chip bearing component structures faces the substrate and bump connections electrically connect the metallization of the substrate with the connection areas provided on the chip provide a slight distance from the substrate; applying a material to cover at least the lower edges of the chip and a region of the substrate abutting the edges of the chip; applying a first, continuous metal layer on the back side of the chip, on the material and on edge regions of the substrate abutting the material; and applying a second, hermetically sealing metal layer by a solvent-free process at least on the regions of the first metal layer that cover the material.

15 22. (New) A method according to claim 21, wherein the step of applying the second metal layer provides a metal foil placed onto the first metal layer and includes heating to melt the metal foil onto the first metal layer.

20 23. (New) A method according to claim 22, wherein the step of providing the metal foil provides a metal foil having contours of the first metal layer so that it lies on the first metal layer with a positive fit.

24. (New) A method according to claim 21, wherein the step of applying the second metal layer applies metal particles and then melts the particles onto the first metal layer.

25 25. (New) A method according to claim 21, wherein the step of applying the second metal layer applies a metal paste and then bakes the paste onto the first metal layer.

26. (New) A method according to claim 21, wherein the step of applying the second metal layer utilizes a process selected from CVD and PVD.

27. (New) A method according to claim 21, wherein the step of applying a second metal layer sputters the second metal layer onto the first metal
5 layer.

28. (New) A method according to claim 21, wherein the step of applying the second metal layer applies the second layer continuously on the first metal layer.

29. (New) A method according to claim 21, which, after applying the
10 first metal layer and before applying the second metal layer, includes removing surface layers of the first metal layer to improve the bonding of the second metal layer thereon.

30. (New) A method according to claim 21, wherein, after the step of applying the first metal layer, removing an oxide layer from the first metal layer
15 via a hydrogen plasma.

31. (New) A method according to claim 21, wherein the step of applying the material applies a plastic film on the back side of the chip to cover the back side, the edges of the chip and subsequently seals the film with the substrate in the entire edge region around the chip.

20 32. (New) A method according to claim 21, wherein the step of applying the second metal layer creates a metal alloy with a melting point greater than 260°C in the boundary surface between the first and second metal layers during the application of the second metal layer.

25 33. (New) A method according to claim 21, wherein the step of applying the second metal layer applies a metal layer of a metal selected from a group consisting of tin, tin-silver, tin-silver copper alloys and mixtures of said metals.

34. (New) A method according to claim 33, wherein the step of applying the first metal layer applies a layer of titanium and a layer of copper on the layer of titanium.

5 35. (New) A method according to claim 34, wherein the heating of the second metal layer produces a tin-copper alloy with a melting point greater than 260°C in the boundary between the first metal layer and the second metal layer.

36. (New) A method according to claim 21, which includes a plurality of chips being applied on the substrate in a spaced manner and said steps of applying material and metal layers applies these to each of said chips.

10 37. (New) A method according to claim 36, which includes, subsequent to applying the second metal layer on the chips, isolating the individual components by sectioning between the chips outside of the edge regions of each component.

15 38. (New) A method according to claim 37, wherein the step of applying the first metal layer applies a titanium layer and then a copper layer on each of the components, the step of applying the second metal layer applies a tin layer on the first metal layer, said step of sectioning including removing the second metal layer in the regions to be sectioned to expose the first metal layer, chemically etching the exposed regions of the first metal layer to remove the exposed portions 20 and subsequently sectioning by sawing the components apart.

39. (New) A method according to claim 38, wherein the step of chemically etching utilizes an iron chloride solution.

40. (New) A method according to claim 21, wherein the component is a surface wave component.